In the Claims:

1 - 28. [cancelled]

29. [new] A method of identifying faulty programmable interconnect resources of a field programmable gate array during normal on-line operation comprising the steps of:

configuring said field programmable gate array into an initial self-testing area and a working area, said working area maintaining normal operation of the field programmable gate array;

testing at least two groups of wires under test located within said self-testing area for faults;

identifying a faulty group of wires under test from said at least two groups of wires under test having a faulty programmable interconnect resource therein;

minimizing a region of said faulty group of wires under test containing said faulty programmable interconnect resource;

identifying a wire within said faulty group of wires under test containing said faulty programmable interconnect resource;

replacing programmable interconnect resources within said wire and said region with fault-free programmable interconnect resources for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

30. [new] The method set forth in claim 29, wherein the step of minimizing a region of said faulty group of wires under test containing said faulty programmable interconnect resource includes establishing said programmable interconnect resources located within said initial self-testing area as at least two subsequent groups of wires under test, at least one of said subsequent groups including a

subdivided portion of said programmable interconnect resources located within said faulty group of wires under test; and

testing said at least two subsequent groups of wires under test for faults in order to determine which subsequent group of wires under test includes said faulty programmable interconnect resource.

31. [new] The method set forth in claim 30, wherein the steps of establishing and testing are repeated until the region of said faulty group of wires under test which includes said faulty resource is minimized.

32. [new] The method set forth in claim 31, wherein the step of identifying a wire within said faulty group of wires under test containing said faulty programmable interconnect resource includes establishing said programmable interconnect resources located within said initial self-testing area as at least two wires under test, at least one of said wires including a subdivided portion of said minimized region of said faulty group of wires under test; and

testing said at least two wires under test for faults in order to determine which wire under test includes said faulty programmable interconnect resource.

33. [new] The method set forth in claim 32, wherein the steps of establishing and testing are repeated until the wire of said minimized region of said faulty group of wires under test which includes said faulty resource is identified.

34. [new] The method set forth in claim 33, wherein the step of replacing programmable interconnect resources within said wire of said minimized region of said faulty group of wires under test to avoid suspect resources includes reconfiguring said programmable interconnect resources located within said initial self-testing area to avoid

suspect faulty wire segments and configuration interconnect points; and

testing said reconfigured wire of said minimized region of said faulty group of wires under test in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

35. [new] The method set forth in claim 34, wherein the steps of reconfiguring and testing are repeated until the faulty programmable interconnect resource of said wire of said minimized region of said faulty group of wires under test is identified.

36. [new] The method set forth in claim 35 further comprising the step of roving said initial self-testing area by reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area.

37. [new] The method set forth in claim 29, wherein the step of identifying a wire within said faulty group of wires under test containing said faulty programmable interconnect resource includes establishing said programmable interconnect resources located within said initial self-testing area as at least two wires under test, at least one of said wires including a subdivided portion of said faulty group of wires under test; and

testing said at least two wires under test for faults in order to determine which wire under test includes said faulty programmable interconnect resource.

38. [new] The method set forth in claim 37, wherein the steps of establishing and testing are repeated until the wire of said faulty group of wires under test which includes said faulty resource is identified.

39. [new] The method set forth in claim 38, wherein the step of minimizing a region of said faulty group of wires under test containing said faulty programmable interconnect resource includes establishing said programmable interconnect resources located within said initial self-testing area as at least two subsequent wires under test, at least one of said subsequent wires under test including a subdivided portion of said programmable interconnect resources located within said faulty wire under test; and

testing said at least two subsequent wires under test for faults in order to determine which subsequent wire under test includes said faulty programmable interconnect resource.

40. [new] The method set forth in claim 39, wherein the steps of establishing and testing are repeated until the region of said faulty wire under test which includes said faulty resource is minimized.

41. [new] The method set forth in claim 40, wherein the step of replacing programmable interconnect resources within said wire of said minimized region of said faulty group of wires under test to avoid suspect resources includes reconfiguring said programmable interconnect resources located within said initial self-testing area to avoid suspect faulty wire segments and configuration interconnect points; and

testing said reconfigured wire of said minimized region of said faulty group of wires under test in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

42. [new] The method set forth in claim 41, wherein the steps of reconfiguring and testing are repeated until the faulty programmable interconnect resource of said wire of said minimized region of said faulty group of wires under test is

identified.

43. [new] The method set forth in claim 42 further comprising the step of roving said initial self-testing area by reconfiguring said field programmable gate array such that a portion of said working area becomes a subsequent self-testing area and at least a portion of said initial self-testing area becomes a portion of said working area.

44. [new] The method set forth in claim 36, wherein the step of identifying a faulty group of wires under test from said at least two groups of wires under test includes propagating test patterns along at least two groups of wires under test;

comparing outputs of said at least two groups of wires under test; and

producing fault status data for said at least two groups of wires under test.

45. [new] The method set forth in claim 43, wherein the step of identifying a faulty group of wires under test from said at least two groups of wires under test includes propagating test patterns along at least two groups of wires under test;

comparing outputs of said at least two groups of wires under test; and

producing fault status data for said at least two groups of wires under test.

46. [new] An apparatus for identifying faulty programmable interconnect resources of a field programmable gate array comprising:

a controller in communication with the field programmable gate array for: (a) configuring the field programmable gate array into a self-testing area and a working area, the working area maintaining normal operation of the field programmable gate array; (b) initiating testing of at least two groups of wires under test located within said self-testing area for faults; (c) identifying a faulty group of wires under test from said at least two groups of wires under test having a faulty programmable interconnect resource

therein; (d) minimizing a region of said faulty group of wires under test containing said faulty programmable interconnect resource; (e) identifying a wire within said faulty group of wires under test containing said faulty programmable interconnect resource; and (f) replacing programmable interconnect resources within said wire and said region with fault-free programmable interconnect resources for further testing in order to identify a wire segment, a configuration interconnect point, and/or a combination thereof which includes said fault.

47. [new] The apparatus for identifying faulty programmable interconnect resources of a field programmable gate array of claim 46, further comprising a storage medium in communication with said controller for storing a functional configuration of the field programmable gate array, a plurality of test configurations, and fault status data.

48. [new] The apparatus for identifying faulty programmable interconnect resources of a field programmable gate array of claim 47, wherein said self-testing area roves by reconfiguring the field programmable gate array such that a portion of the working area becomes a subsequent self-testing area and at least a portion of the initial self-testing area becomes a portion of the working area.